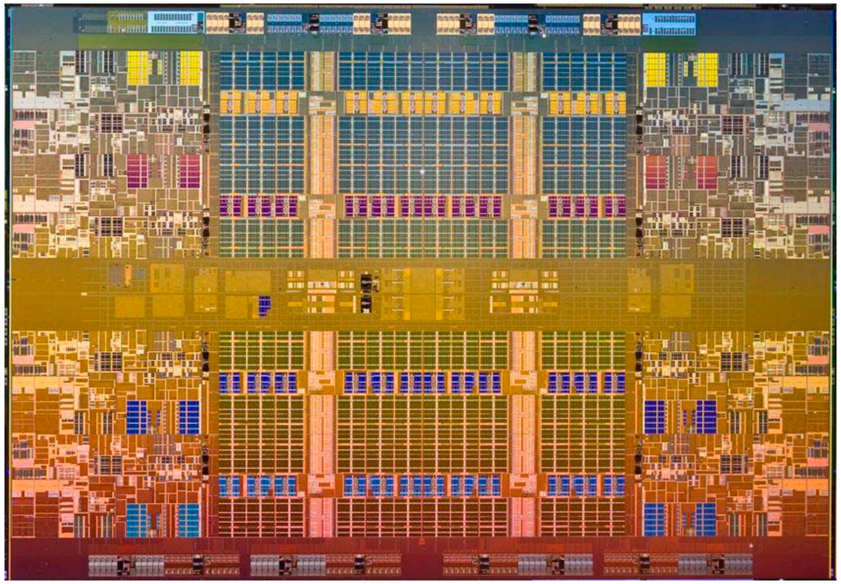
A Comprehensive Review of the Challenges and Opportunities Confronting Cache Memory System Performance


Photograph of Intel Xeon processor 7500 series die showing cache memories [1]

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300% !

That's one estimate of how much a processor's core bandwidth requirements *exceed* the ability of the cache to supply data

[2,3]

Challenges Confronting Cache Memory System Performance

Some additional astonishing facts…

x30	That's the estimated required increase in cache memory bandwidth that is required for every x10 increase in processor transistor count.
50%	That's the estimated impact that cache memory has on the overall computer architecture's power requirements.
#1	… in cost. Cache memory is said to be the most expensive memory in the overall computer system.

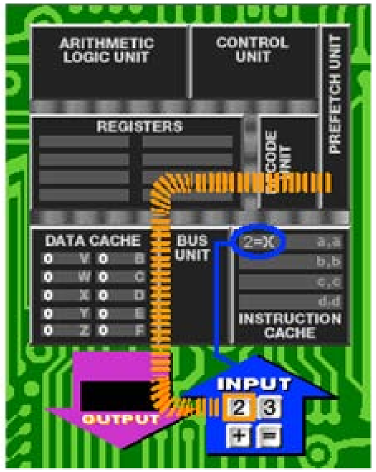
And many of those estimates were predicted over 30 years ago!

[2,3,4,5]

Today's Objectives and Contributions

To take you to the forefront of cache memory research opportunities to improve performance

- Advances in Cache Data Management: Prefetching, Bandwidth Management, Scheduling, and Data Placement (Abhishek Ramamurthy)
- Energy Efficiency Opportunities (Mathias Elmlinger)
- Advanced Topics in Cache Memory Research (Pranav Timmireddy)

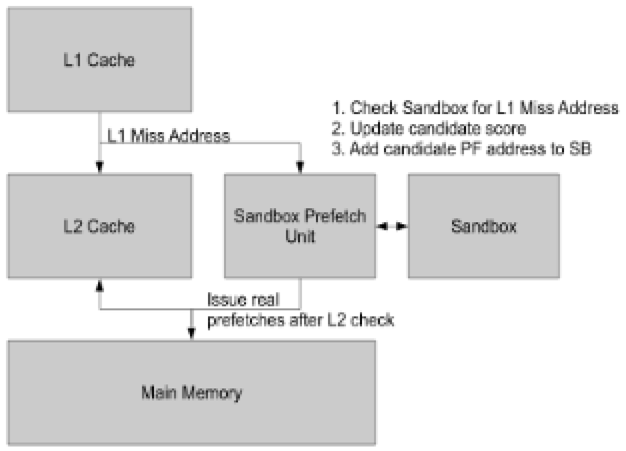


Advances in Cache Data Management: Prefetching, Bandwidth Management, and Data Placement

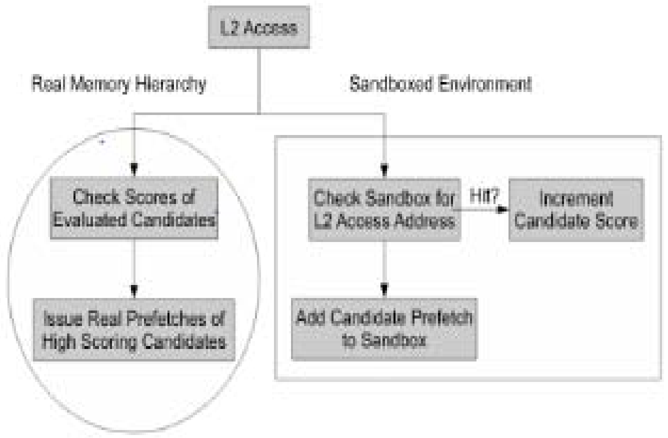
- Why is it necessary to have cache prefetching?
- What is the bottle neck involved in prefetching data from cache memory?
- How to improve the cache memory density?

Sandbox Prefetching Mechanism

- Technique is based on bloom filter (Howard Bloom, 1970).


L1 Cache
L1 Miss Address
1. Check Sandbox for L1 Miss Address
2. Update candidate score
3. Add candidate PF address to SB
L2 Cache
Sandbox Prefetch Unit
Sandbox
Issue real prefetches after L2 check
Main Memory

Sandbox Prefetch Architecture [14]

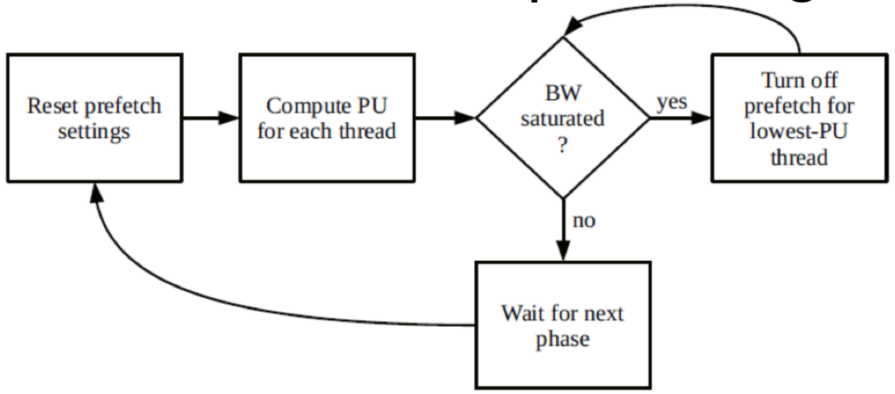

L2 Access
Real Memory Hierarchy
Sandboxed Environment
Check Scores of Evaluated Candidates
Issue Real Prefetches of High Scoring Candidates
Check Sandbox for L2 Access Address
Hit?
Increment Candidate Score
Add Candidate Prefetch to Sandbox

Sandbox Prefetch Action on L2 Access [14]

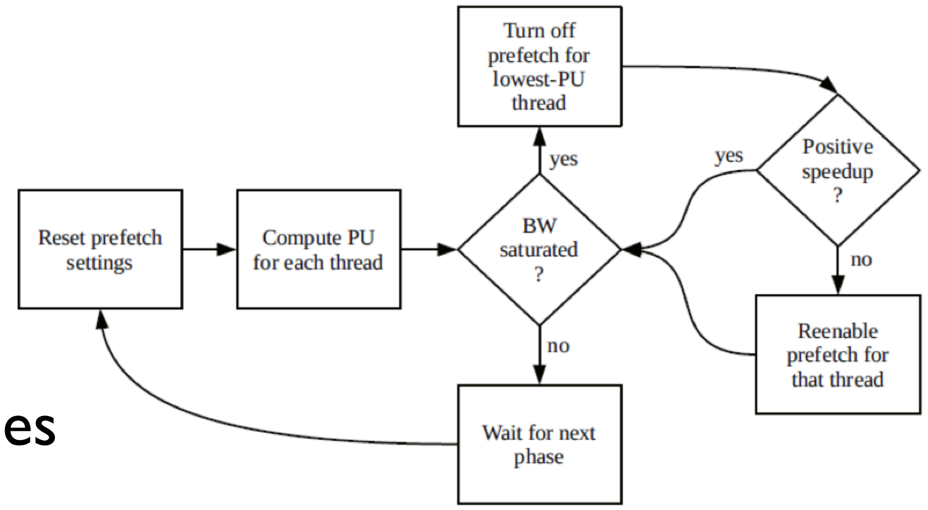
- SandBox Prefetching (SBP) improves Address Mapped Pattern Matching performance by 3.9% in a multicore environment.

Increasing Multicore Efficiency through Intelligent Bandwidth Shifting

- Technique provides better efficiency through assigning bandwidth for prefetching based on prefetch efficiency.


Reset prefetch settings
Compute PU for each thread
BW saturated ?
yes
Turn off prefetch for lowest-PU thread
no
Wait for next phase

Base Bandwidth shifting algorithm [16]

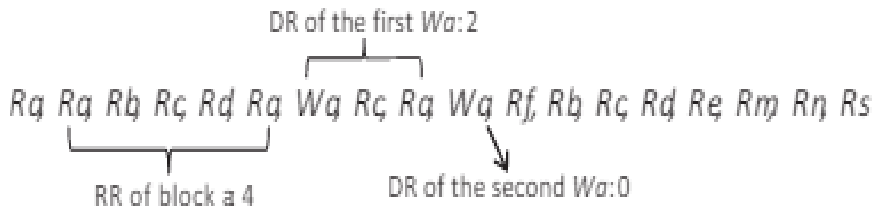

Turn off prefetch for lowest-PU thread
Positive speedup ?
yes
yes
Reset prefetch settings
Compute PU for each thread
BW saturated ?
no
no
Reenable prefetch for that thread
Wait for next phase

- Improved multicore efficiencies by 7% for random workloads.

Modified Base Bandwidth shifting algorithm [16]

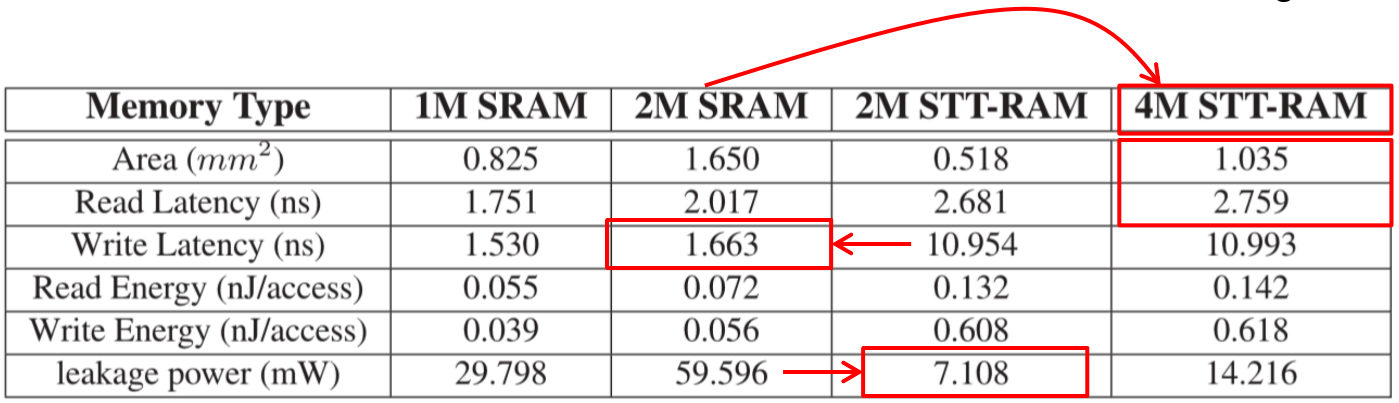
Adaptive Placement Policies for Data in Cache Memory Systems

- The technique provides a better way placing most frequently used data in cache and evicting the least used data block in cache.



Read range and Depth Range[17]

2x more storage AND ~60% less area



Memory Type	1M SRAM	2M SRAM	2M STT-RAM	4M STT-RAM
Area (mm^2)	0.825	1.650	0.518	1.035
Read Latency (ns)	1.751	2.017	2.681	2.759
Write Latency (ns)	1.530	1.663	10.954	10.993
Read Energy (nJ/access)	0.055	0.072	0.132	0.142
Write Energy (nJ/access)	0.039	0.056	0.608	0.618
leakage power (mW)	29.798	59.596	7.108	14.216

Area and read / write latency of SRAM and STT-RAM [17]

Energy Efficiency

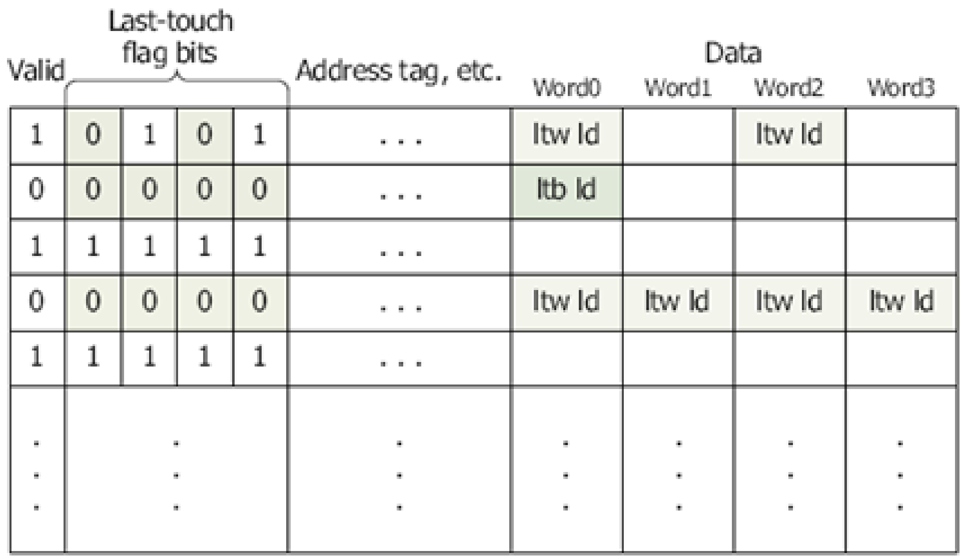
- Crucial factor: energy efficiency

- Why cache?
  - Large fraction of chip size
  - Estimated: 50% of energy dissipation by cache

- Approaches to improve energy efficiency
  - Software Self Invalidation (L1) and Data Compression (L2)
  - Exploiting row access locality (DRAM)
  - Improve Error Correcting Codes and Error Detection Codes (L1)
  - Isolation nodes and dynamic memory partitioning techniques (L1/L2)

Energy Efficiency
Software Self-Invalidation and Data Compression

- Invalidation
  - Through request
  - Last-touch load/store instructions

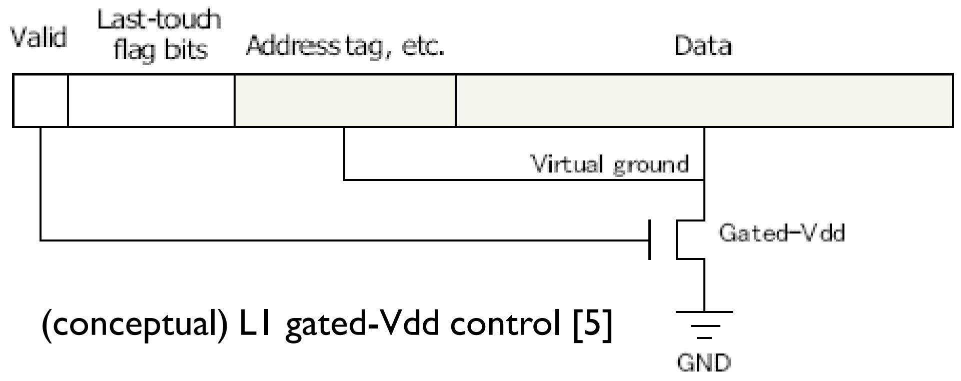


Valid	Last-touch flag bits				Address tag, etc.	Data			
						Word0	Word1	Word2	Word3
1	0	1	0	1	. . .	ltw ld		ltw ld	
0	0	0	0	0	. . .	ltb ld			
1	1	1	1	1	. . .				
0	0	0	0	0	. . .	ltw ld	ltw ld	ltw ld	ltw ld
1	1	1	1	1	. . .				
⋮	⋮				⋮	⋮	⋮	⋮	⋮

L1 cache memory structure [5]

Energy Efficiency
Software Self-Invalidation and Data Compression

- Invalidation
  - Through request
  - Last-touch load/store instructions

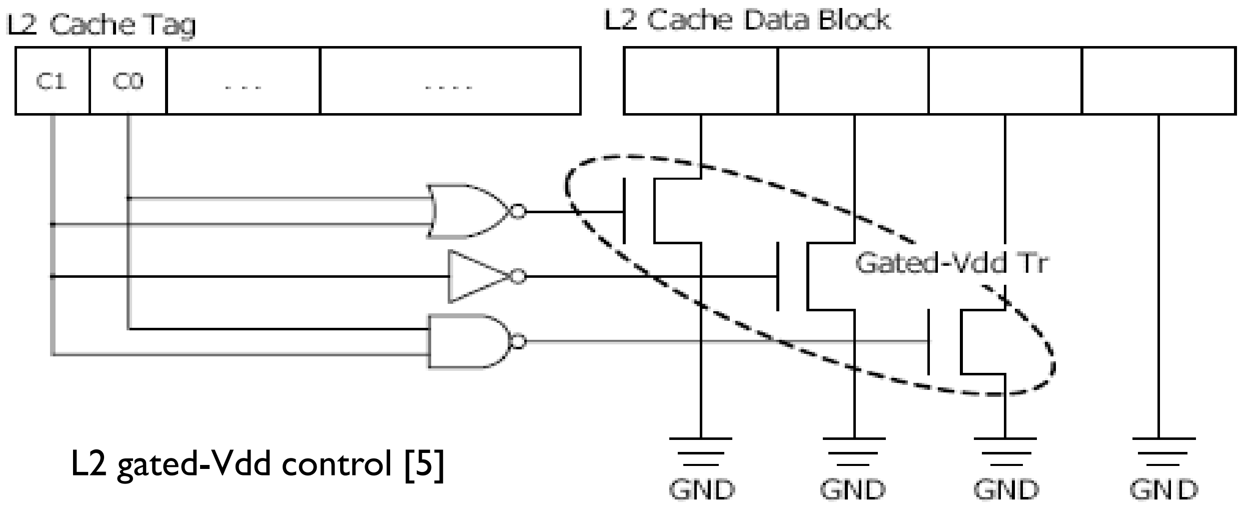


(conceptual) L1 gated-Vdd control [5]

- Reduction of up to 10% in terms of leakage energy

Energy Efficiency
Software Self-Invalidation and Data Compression

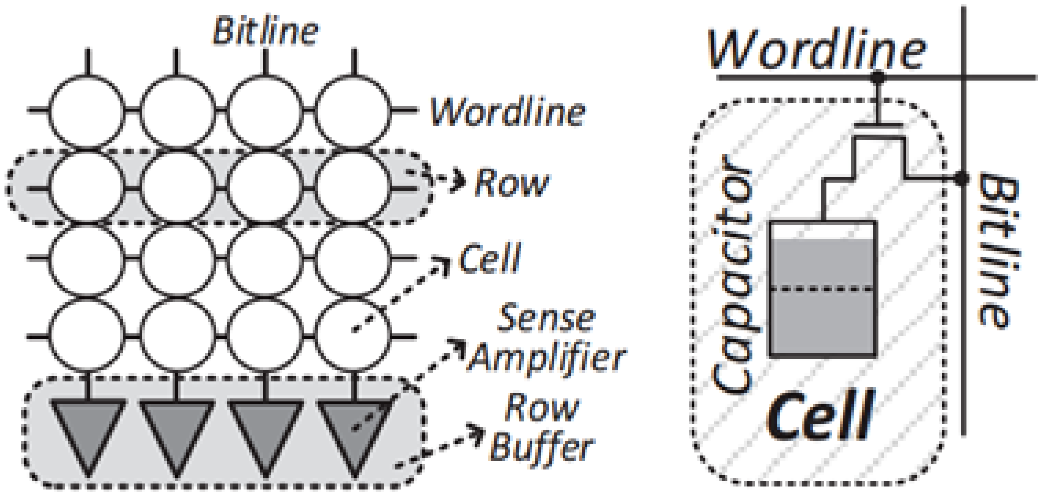
- Data compression
  - Less memory space used
  - More memory space can be turned off



L2 gated-Vdd control [5]

- Reduction of up to 25% in terms of leakage energy

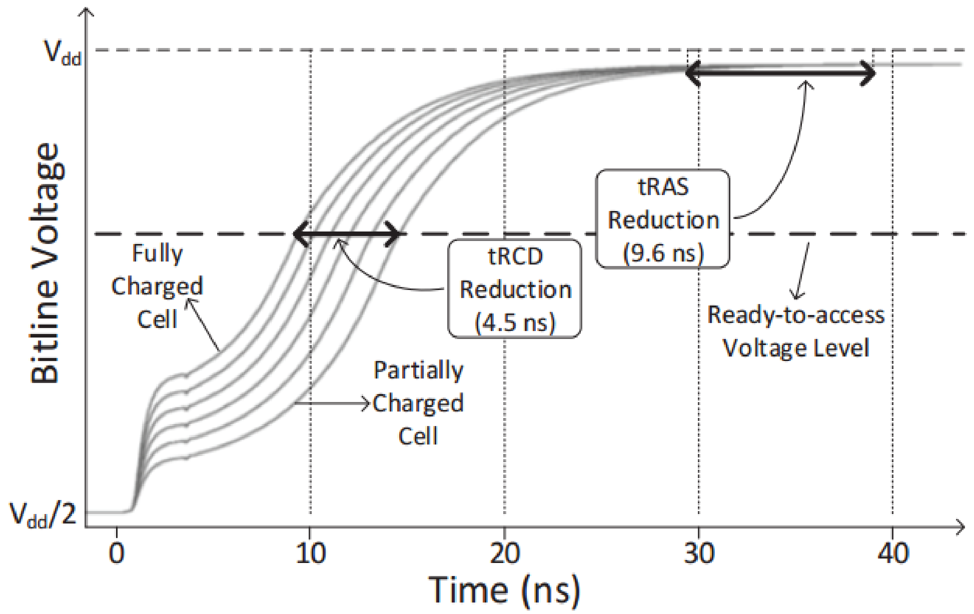
Energy Efficiency
Exploiting Row Access Locality



DRAM Sub-Array (left) and DRAM cell (right) [6]

- Timing to access rows based on amount of charge
- Keep track of charge of recently accessed rows
  - Table in main memory controller
  - Hit: lower timing parameters

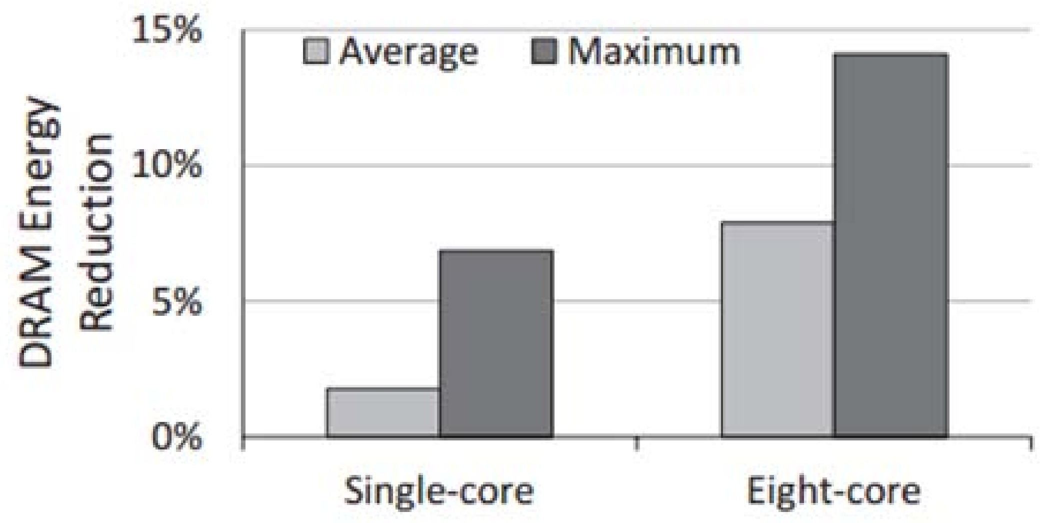
Energy Efficiency
Exploiting Row Access Locality



Effect of initial cell charge on bit line voltage [6]

- Timing to access rows based on amount of charge
- Keep track of charge of recently accessed rows
  - Table in main memory controller
  - Hit: lower timing parameters

Energy Efficiency
Exploiting Row Access Locality



DRAM energy reduction of ChargeCache [6]

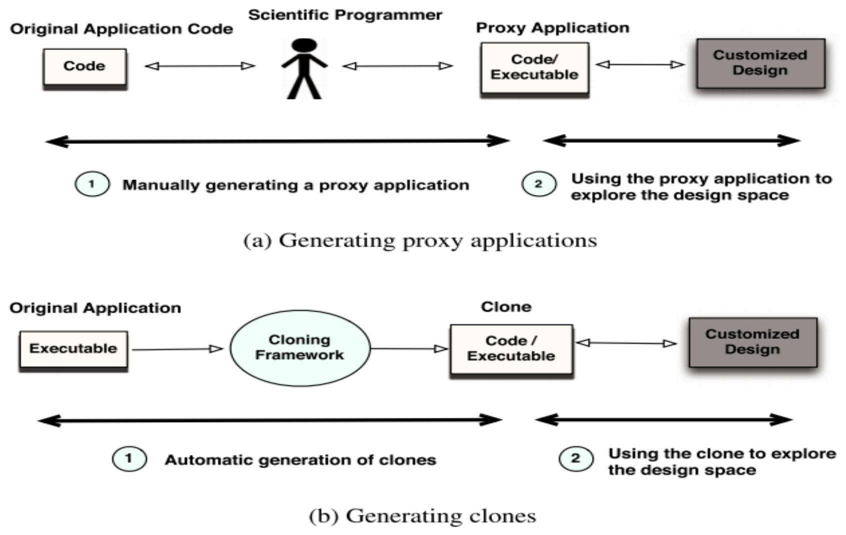
- Single-core: 1.8% average (max. 6.9%)
- Eight-core: 7.9% average (max. 14.1%)

Advanced Topics in Cache Memory Research

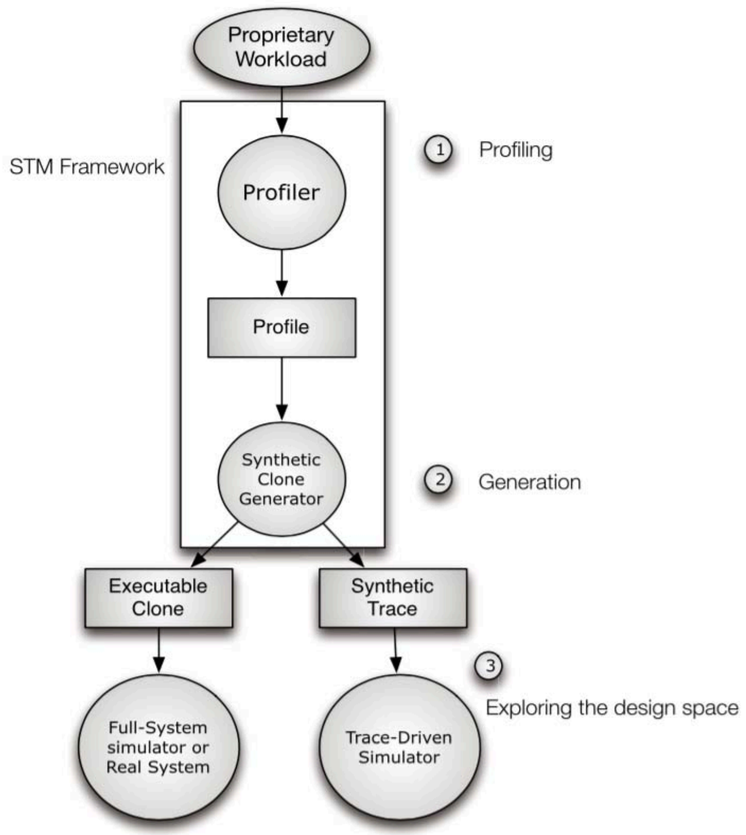
- STM : Cloning the Spatial and Temporal Memory Access Behavior
- RADAR (Runtime- Assisted Dead Region) Management for Last Level Caches

STM: Spatial and Temporal Cloning

- Transition probability table indexed by stride history pattern is used to capture the spatial locality
- A combination of stack distance profile and stride pattern table

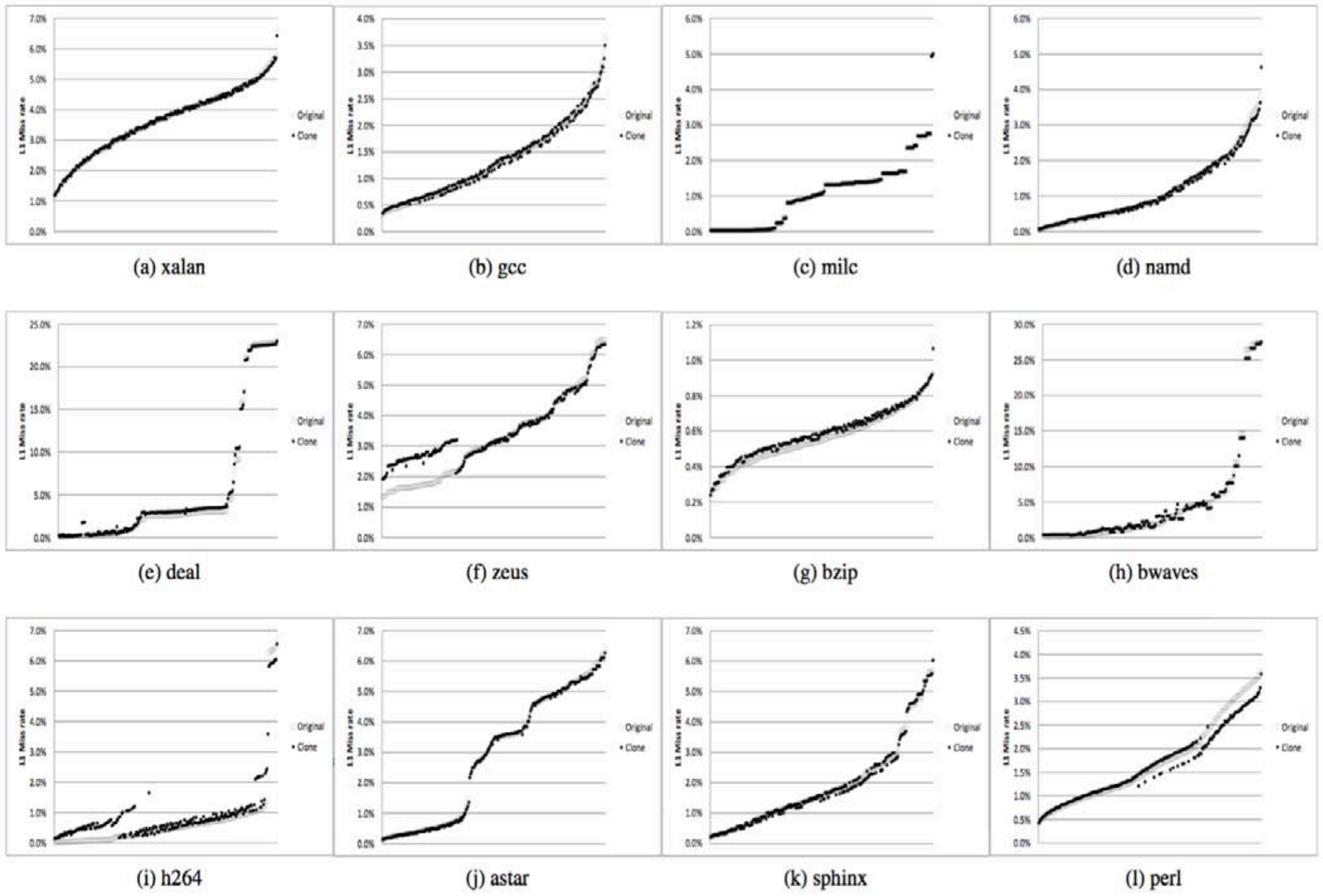

Original Application Code
Scientific Programmer
Proxy Application
Code
Code/ Executable
Customized Design
1 Manually generating a proxy application
2 Using the proxy application to explore the design space
(a) Generating proxy applications
Original Application
Clone
Executable
Cloning Framework
Code / Executable
Customized Design
1 Automatic generation of clones
2 Using the clone to explore the design space
(b) Generating clones

Proxy application versus cloning [19]



STM Framework [19]

STM – Cont'd

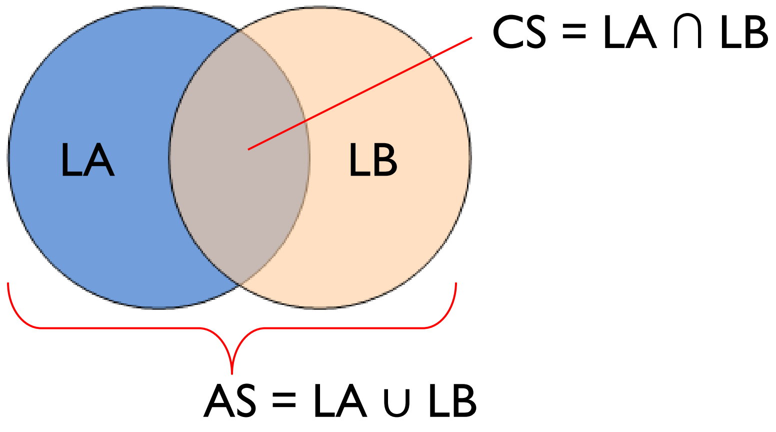


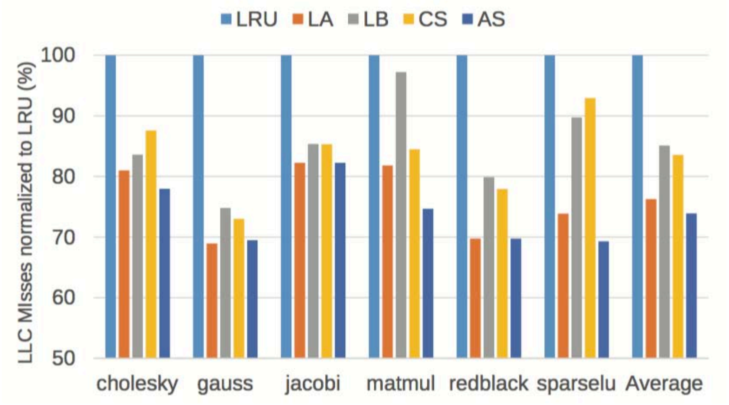
STM on different benchmarks [19]

Original vs clone L1 miss rate across different cache prefetchers and configurations

RADAR: Runtime- Assisted Dead Region Management

- Efficient management of LLCs is essential
- Existing protocols use either dynamic or static techniques.
- RADAR is a hybrid static/dynamic technique which improves LLC efficiency.
- Look Ahead (LA), Look Back (LB), Conservative combined Scheme (CS = LA ∩ LB), Aggressive combined Scheme (AS = LA ∪ LB).





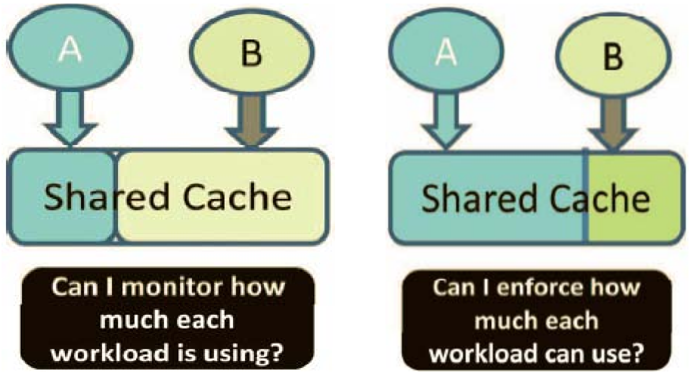
LLC miss rate for different RADAR [21]

- Aggressive Combined scheme performs best and more than 26% reduction in LLC misses over the baseline LRU.

Taking Research into Reality

Such opportunities do translate into results.

An example: two cache bandwidth Quality of Service concepts called CMT (Cache Monitoring Technology) and CAT (Cache Allocation Technology) took over 10 years to go from research to silicon.


A
B
Shared Cache
Can I monitor how much each workload is using?
A
B
Shared Cache
Can I enforce how much each workload can use?

Overview of CMT (Left) and CAT (Right) [24]

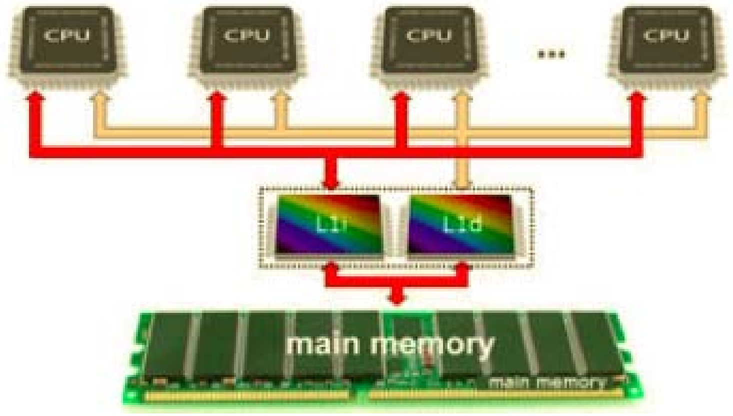
On June 4, 2013, Intel introduced the Xeon "Haswell" 4th generation processor employing both CMT and CAT technologies [29].

…. providing as high as a <u>450%</u> improvement [24].

Conclusion and Future Work

While cache memory system advances continue to be made… these advances are consistently offset by the ever increasing requirements for multicore processors.

One estimate is that by 2020, multicore processors will reach *zetta-flop* (10^{21}) speeds [25].



Envisioned optical RAM cache architecture [25]

With such demands, the need for additional breakthroughs in the area of cache memory architectures remains critical.

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Questions?

THANK YOU!